| Notice of References Cited | Application/Control No. 10/721,573 | Applicant(s)/Patent Under Reexamination LOONG, LOW YAU | |
|---|---|---|---|
| | Examiner Phallaka Kik | Art Unit 2825 | Page 1 of 3 |

**U.S. PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| | A | US-6,594,808 | 07-2003 | Kale et al. | 716/8 |
| | B | US-5,359,537 | 10-1994 | Saucier et al. | 716/18 |
| | C | US-2002/0178432 | 11-2002 | Kim et al. | 716/18 |
| | D | US-6,148,433 | 11-2000 | Chowdhary et al. | 716/1 |
| | E | US-6,289,488 | 09-2001 | Dave et al. | 716/1 |
| | F | US-2003/0182645 | 09-2003 | Fairbanks, Brent Alan | 716/5 |
| | G | US-6,832,357 | 12-2004 | Saluja et al. | 716/2 |
| | H | US-6,601,221 | 07-2003 | Fairbanks, Brent Alan | 716/5 |
| | I | US-6,080,204 | 06-2000 | Mendel, David Wolk | 716/7 |
| | J | US-6,038,386 | 03-2000 | Jain, Gitu | 716/16 |
| | K | US-5,974,242 | 10-1999 | Damarla et al. | 716/2 |
| | L | US-5,610,829 | 03-1997 | Trimberger, Stephen M. | 716/16 |
| | M | US-5,461,577 | 10-1995 | Shaw et al. | 716/17 |

**FOREIGN PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | Classification |
|---|---|---|---|---|---|---|
| | N | | | | | |
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| | S | | | | | |
| | T | | | | | |

**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | Chen et al., "A New Strategy of Performance-Directed Technology Mapping Algorithm for LUT-Based FPGAs", 1996 IEEE International Symposium on Circuits and Systems, Vol. 4, 12-15 May 1996, pp. 822-825. |
| | V | Yan, "Logic Synthesis for CPLDs and FPGAs with PLA-Style Logic Blocks", Fourteenth International Conference on VLSI Design, 3-7 January 2001, pp. 291-297. |
| | W | Chattopadhyay et al., "KGPMAP: Library-Based Technology-Mapping Technique for Antifused Based FPGAs", IEE Proceedings of Computers and Digital Techniques, Vol. 141, No. 6, November 1994, pp. 361-368. |
| | X | Brasen et al., "Using Cone Structures for Circuit Partitioning into FPGA Packages", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 17, No. 7, July 1998, pp 592-600. |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

| Notice of References Cited | Application/Control No. 10/721,573 | Applicant(s)/Patent Under Reexamination LOONG, LOW YAU | |
|---|---|---|---|
| | Examiner Phallaka Kik | Art Unit 2825 | Page 2 of 3 |

**U.S. PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| | A | US-5,128,871 | 07-1992 | Schmitz, Nicholas A. | 716/17 |
| | B | US-4,703,435 | 10-1987 | Darringer et al. | 716/18 |
| | C | US-2004/0133869 | 07-2004 | Sharma, Sunil Kumar | 716/016 |
| | D | US-2004/0088663 | 05-2004 | Wu et al. | 716/006 |
| | E | US-6,622,291 | 09-2003 | Ginetti, Arnold | 716/9 |
| | F | US-5,835,751 | 11-1998 | Chen et al. | 716/16 |
| | G | US-6,336,208 | 01-2002 | Mohan et al. | 716/16 |
| | H | US- | | | |
| | I | US- | | | |
| | J | US- | | | |
| | K | US- | | | |
| | L | US- | | | |
| | M | US- | | | |

**FOREIGN PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | Classification |
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| | N | | | | | |
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| | T | | | | | |

**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | Naseer et al., "Direct Mapping of RTL Structures onto LUT-Based FPGAs", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 17, No. 7, July 1998, pp. 624-631. |
| | V | Mathur et al., "Compression-Relaxation: A New Approach to Timing-Driven Placement for Regular Architectures", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No. 6, June 1997, pp. 597-608. |
| | W | Cong et al., "Simultaneous Depth and Area Minimization in LUT-Based FPGA Mapping", Proceedings of the Third International ACM Symposium on Field-Programmable Gate Arrays, 1995, pp. 68-74. |
| | X | Francis et al., "Chortle: A Technology Mapping Program for Lookup Table-Based Field Programmable Gate Arrays", Proceedings of 27th ACM/IEEE Design Automation Conference, 24-28 June 1990, pp. 613-619. |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

| Notice of References Cited | Application/Control No. 10/721,573 | Applicant(s)/Patent Under Reexamination LOONG, LOW YAU | |
|---|---|---|---|
| | Examiner Phallaka Kik | Art Unit 2825 | Page 3 of 3 |

**U.S. PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| | A | US- | | | |
| | B | US- | | | |
| | C | US- | | | |
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**FOREIGN PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | Classification |
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| | T | | | | | |

**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | NN81081455, "Conversion of PLA-Logic Implementations", IBM Technical Disclosure Bulletin, Vol. 24, No. 3, August 1981, pp. 1455-1456 (4 pages). |
| | V | Schlag et al., "Empirical Evaluation of Multilevel Logic Minimization Tools for a Lookup-Table-Based Field-Programmable Gate Array Technology," IEEE Transactions on Computer-Aided Design of ICs and Systems, Vol. 12, No. 5, May 1993, pp. 713-722. |
| | W | Her et al., "A PLA-Based Algorithm for Estimating Transition Densities in Two-Level Combinational Logic Circuits", 1994 IEEE Asia-Pacific Conference on Circuits and Systems, 5-8 December 1994, pp. 448-453. |
| | X | Ruan et al., "Synthesis of Partition-Codec Architecture for Low Power and Small Area Circuit Design", The 2001 IEEE International Symposium on Circuits and Systems, Vol. 5, 6 May 2001, pp. 523-526. |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.